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1. A method to design and verify a multi-power integrated circuit device comprising:

providing a multi-power gate-level netlist comprising
multi-power net information;

translating said multi-power gate-level netlist to

thereby create a non-multi-power gate-level netlist wherein
said translating comprises removing said multi-power net
information;

placing and routing circuit cells to create a physical view of said multi-power integrated circuit device wherein said placing and routing uses said non-multi-power gate-level netlist and wherein text labels for said multi-power net information are attached to said physical view; and

comparing said physical view and said multi-power gate level netlist to verify the correctness of said physical view and to complete said design and verification of said multi-power integrated circuit device.

2. The method according to Claim 1 wherein said multi-power integrated circuit device comprises input/output (I/O) cells having multiple power supplies.

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- 3. The method according to Claim 2 wherein said multiple power supplies comprise a first supply of between about 2.5 Volts and a second supply of about 3.3 Volts.
- 4. The method according to Claim 1 wherein said multi-power integrated circuit device comprises analog circuits and digital circuits.
 - 5. The method according to Claim 1 wherein said step of placing and routing further comprises clock tree synthesis (CTS) placement and routing.
 - 6. The method according to Claim 1 further comprising:

clock tree synthesized (CTS) placing and routing of said circuit cells after said step of placing and routing circuit cells to create a physical view of said multi-power integrated circuit device wherein said CTS placing and routing updates said physical view and modifies said non-multi-power gate-level netlist to thereby create a CTS modified non-multi-power gate-level netlist; and

inserting said includes multi-power net information

10 into said CTS modified non-multi-power gate-level netlist
to create an updated said multi-power gate-level netlist
prior to said step of comparing said physical view and said

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multi-power gate-level netlist to verify the correctness of said physical view and to complete said design and

verification of said multi-power integrated circuit device.

- 7. The method according to Claim 6 further comprising:

 comparing said multi-power gate-level netlist and said

 updated multi-power gate-level netlist to thereby verify

 that no errors have been introduced after said step of

 inserting said includes multi-power net information into

 said CTS modified non-multi-power gate-level netlist.
- 8. The method according to Claim 1 further comprising:

 simulating said multi-power gate-level netlist; and
 thereafter performing static timing analysis on said
 multi-power gate-level netlist prior to said step of
 providing said multi-power gate-level netlist.
 - 9. A method to design and verify a multi-power integrated circuit device comprising:

providing a multi-power gate-level netlist wherein said multi-power gate-level netlist includes multi-power net information;

translating said multi-power gate-level netlist to thereby create a non-multi-power gate-level netlist wherein

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said translating comprises removing said multi-power net information;

placing and routing circuit cells to create a physical view of said multi-power integrated circuit device wherein said placing and routing uses said non-multi-power gate-level netlist and wherein text labels for said multi-power net information are attached to said physical view;

clock tree synthesized (CTS) placing and routing of said circuit cells after said step of placing and routing circuit cells to create a physical view of said multi-power integrated circuit device wherein said CTS placing and routing updates said physical view and modifies said non-multi-power gate-level netlist to thereby create a CTS modified non-multi-power gate-level netlist;

inserting said includes multi-power net information into said CTS modified non-multi-power gate-level netlist to create an updated said multi-power gate-level netlist; and comparing said physical view and said updated multi-power gate-level netlist to verify the correctness of said physical view and to complete said design and verification of said multi-power integrated circuit device.

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- 10. The method according to Claim 9 wherein said multipower integrated circuit device comprises input/output
 (I/O) cells having multiple power supplies.
- 11. The method according to Claim 10 wherein said multiple power supplies comprise a first supply of between about 2.5 Volts and a second supply of about 3.3 Volts.
- 12. The method according to Claim 9 wherein said multipower integrated circuit device comprises analog circuits
 and digital circuits.
- 13. The method according to Claim 9 further comprising:

 comparing said multi-power gate-level netlist and said

 updated multi-power gate-level netlist to thereby verify

 that no errors have been introduced after said step of

 inserting said includes multi-power net information into

 said CTS modified non-multi-power gate-level netlist.
- 14. The method according to Claim 9 further comprising:

 simulating said multi-power gate-level netlist; and
 thereafter performing static timing analysis on said
 multi-power gate-level netlist prior to said step of
 providing said multi-power gate-level netlist.

15. An apparatus to design and verify a multi-power integrated circuit device comprising:

a means of storing a multi-power gate-level netlist that is provided;

a means of translating said multi-power gate-level netlist to thereby create a non-multi-power gate-level netlist wherein said means of translating comprises removal of said multi-power net information;

a means of placing and routing circuit cells to create

10 a physical view of said multi-power integrated circuit

device wherein said means of placing and routing uses said

non-multi-power gate-level netlist and wherein text labels

for said multi-power net information are attached to said

physical view; and

a means of comparing said physical view and said multi-power gate-level netlist to thereby verify the correctness of said physical view and to complete said design and verification of said multi-power integrated circuit device.

16. The apparatus according to Claim 15 wherein said means of translating comprises a software program running on a computer processing unit.

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- 17. The apparatus according to Claim 15 wherein said means of comparing comprises a logic versus schematic (LVS) software program running on a computer processing unit.
- 18. The apparatus according to Claim 15 further comprising:

 a means of performing a clock tree synthesized (CTS)

 placing and routing of said circuit cells to create a

 physical view of said multi-power integrated circuit device

 wherein said means of performing CTS placing and routing

 updates said physical view and modifies said non-multi
 power gate-level netlist to thereby create a CTS modified

 non-multi-power gate-level netlist; and
- a means of inserting said multi-power net information

 into said CTS modified non-multi-power gate-level netlist

 to create an updated said multi-power gate-level netlist

 for use by said means of comparing said physical view and

 said multi-power gate-level netlist to verify the

 correctness of said physical view and to complete said

 design and verification of said multi-power integrated

 circuit device.
 - 19. The apparatus according to Claim 18 further comprising a means of comparing said multi-power gate-level netlist

and said updated multi-power gate-level netlist to thereby verify that no errors have been introduced.

20. The apparatus according to Claim 15 further comprising a means of displaying said physical view of said multipower integrated circuit device.